CROSSLINK-NX™

MIPI Bridging and Edge AI Combined Into One FPGA

Built on the 28 nm FD-SOI Lattice Nexus platform, the CrossLink-NX family of FPGAs lead their class in power, small form factor, reliability, and performance. They are optimized for a wide range of applications, including embedded vision.

The CrossLink-NX applications include sensor and display bridging, sensors aggregation, sensor duplication, and AI inferencing at the Edge.

Key Features

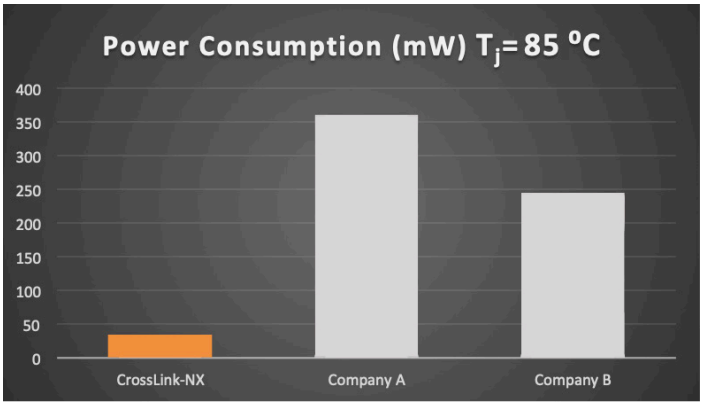
- Low Power
  - Up to 75% lower power vs. competition
- Smallest Form Factor
  - 10x smaller than competition
  - Package sizes as small as 16 mm^2
- High Reliability
  - 100X better Soft Error Rate (SER) vs. competitive offerings
- High Performance
  - Two – 10 Gbps MIPI D-PHY / 2.5 Gbps per D-PHY lane
  - 5 Gbps PCIe
  - 1.5 Gbps differential I/O
  - Ultra-Fast Configuration
    - IO configuration in 3 ms
    - Full device configuration in as low as 8 ms
- Flexible
  - Accelerate AI processing
    - Highest memory to LC ratio (170 bits/LC)
  - Available in Commercial, Industrial and Automotive (AEC-Q100) temperature grades

Device	LIFCL-17	LIFCL-40
Logic Cells	17k	39k
Embedded Memory (EBR) kbits	432	1,512
Large Memory (LRAM) kbits	2560	1024
18 x 18 Multipliers	24	56
ADC Blocks	2	2
GPLL	2	3
Hardened 10 Gbps D-PHY Quads	2	2
Hardened 2.5 Gbps D-PHY Data Lanes (total)	8	8
5 Gbps PCIe	—	1
Temperature Grades[1]	C, I, A	C, I, A
Packages	**Total I/O (Wide Range, High Performance) (D-PHY, PCIe)**	
72 wlcsp (3.7 x 4.1 mm, 0.4 mm)	36 (16, 20) (2, 0)	—
72 QFN (10 x 10 mm, 0.5 mm)	40 (18, 22) (1, 0)	40 (18, 22) (1, 0)
121 csfBGA (6 x 6 mm, 0.5 mm)[2]	72 (24, 48) (2, 0)	72 (24, 48) (2, 0)
256 caBGA (14 x 14 mm, 0.8 mm)[2]	72 (24, 48) (2, 0)	152 (78, 74) (2, 1)
289 csBGA (9.5 x 9.5 mm, 0.5 mm)	—	180 (106, 74) (2, 1)
400 caBGA (17 x 17 mm, 0.8 mm)	—	192 (118, 74) (2, 1)

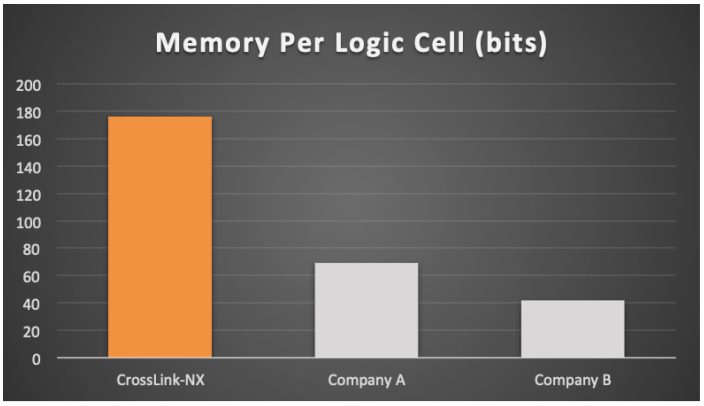
[1] C = Commercial, I = Industrial, A = Automotive
[2] Package available in Automotive grade

Competitive Comparison

Low Power



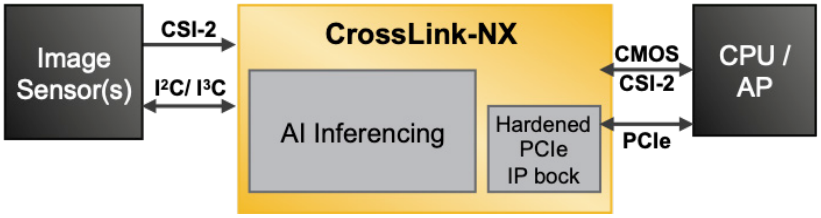
Embedded Memory per LC



Key Applications

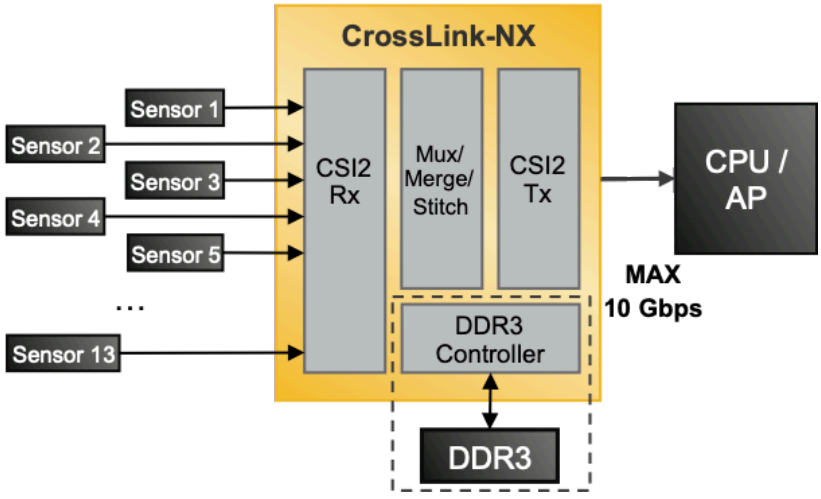
Edge AI Companion

- Bridge one or multiple CSI-2 image sensors to processor interface (PCIe, CMOS, CSI-2)
- Up to 3 Mb of internal RAM for processing
- Offloads inferencing from CPU for object detection / counting
- Combine video bridging and edge AI into a single device



Sensor Aggregation

- Aggregate up to 13 MIPI CSI-2 image sensors into one MIPI CSI-2 output
- Stitch data together into larger horizontal video frame
- Use external DDR memory to stitch data into larger vertical video frame
- Arbitrate data from image sensors using unique virtual channel numbers
- Extend limited processor sensor interface capability and connect more sensors



Applications Support
www.latticesemi.com/support

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